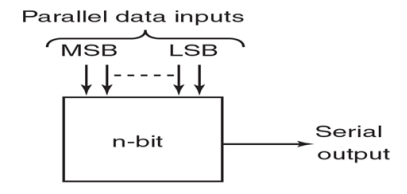
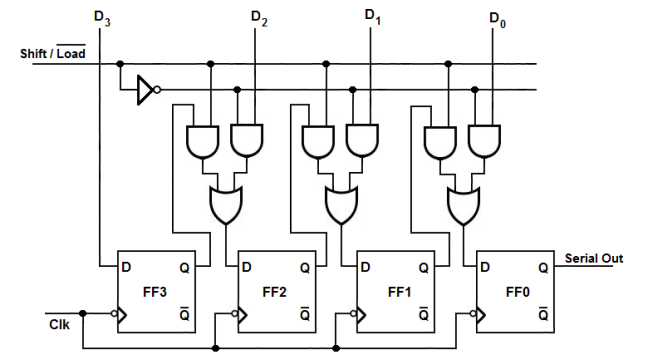
**PISO(Parallel in Serial out) :**

The shift register, which allows parallel input (data is given separately to each flip flop and in a simultaneous manner) and produces a serial output is known as Parallel-In Serial-Out shift register.

The figure below shows the block diagram of PISO shift register

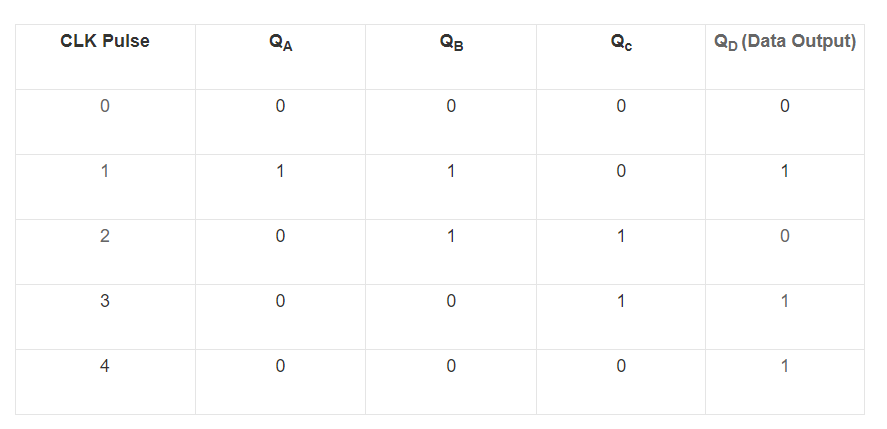


The figure given below shows a 4-bit Parallel In – Serial Out (PISO) shift register which consists of four D flip-flops and an AND-OR logic to determine whether data will load in parallel, or stored data will shift to right.

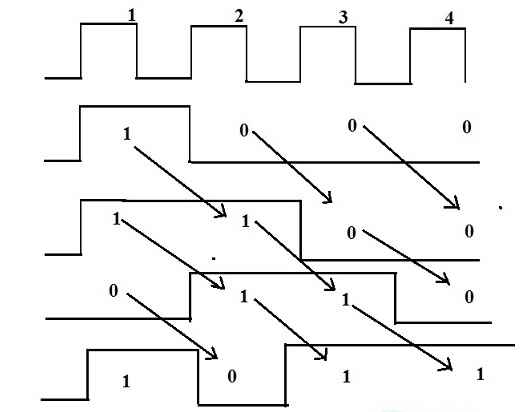


* Here the clock input is directly connected to all the flip flops but the input data is connected individually to each flip flop through a multiplexer at the input of every flip flop.
* The output of the previous flip flop and parallel data input are connected to the input of the MUX and the output of MUX is connected to the next flip flop. All these flip-flops are synchronous with each other since the same clock signal is applied to each flip flop.
* Here shift/load ‘ control line is used to select the functionality of the shift register amongst shift or load at a given instant of time. This is because when the shift/load ‘ line is made low, second **AND** gates of all the combinational circuits become active while first **AND** gates become inactive.
* Thus the bits of the input data word (Data in) appearing as inputs to the second **AND** gates are passed on as the outputs of OR gates at each individual combinational circuit. This causes the individual bits of the Data in to be loaded/stored into respective flip-flops at the appearance of first leading edge of the clock (except the bit **D3** which gets directly stored into FF1 at the first clock tick). This indicates that all the bits of the input data word are stored into the register components at the same clock tick.
* shift/load‘ line is driven high to activate first **and** gates of the combinational circuits which inturn disables the second **and** gates. This causes output bit of each flip-flop to appear at the output of the OR gate driving the very-next flip-flop (except the last flip-flop FF0) At this stage, if the rising edge of the clock pulse appears, then Q1 appears at Q2, Q2 appears at Q3, … and Qn-1 appears at Qn.
* This is nothing but right-shift of the data stored within the register by one-bit. Similarly it is seen that for each of the further clock pulses applied, one bit exits the PISO shift register through the output pin of nth flip-flop (Data out = Qn of FF0), which is nothing but the serial output. Thus one requires n clock cycles to obtain the entire n-bit input data word as a serial output of PISO shift register.

Truth table for parallel in serial out register is given below



Waveform

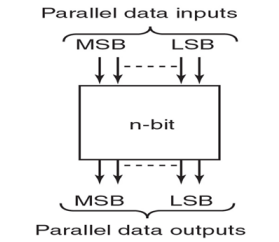


**Why PISO:**

* A PISO shift register is used to change the data from parallel to serial form.
* This kind of shift register is used to generate time delay for digital circuits.
* PISO shift register's practical application is to read numerous switch closures into a chip on a few pins.
* This register reads the data into a memory chip.

**PIPO(Parallel in parallel out):**

**Parallel In Parallel Out (PIPO) shift registers** are the type of storage devices in which both data loading as well as data retrieval processes occur in parallel mode.



**Figure shows Block diagram of PIPO shift register**

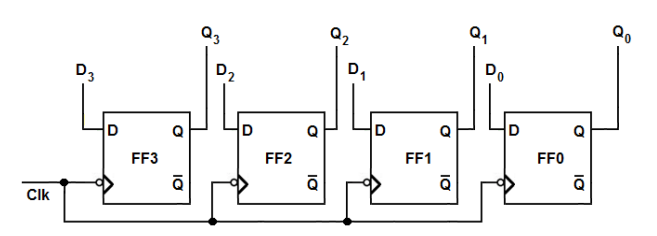
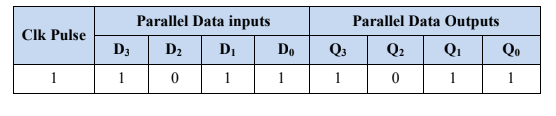
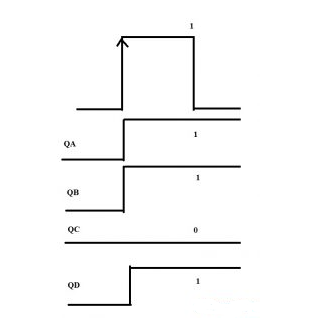
 **4 bit pipo shift register**

Figure shows a PIPO register capable of storing 4-bit input data word (Data in). Here each flip-flop stores an individual bit of the data in appearing as its input (FF3 stores D3 appearing at D; FF2 stores D2 appearing at D; FF1 stores D1 appearing at D1;FF0  stores D0 appearing at D) at the instant of first clock pulse. Further, at the same instant, the bit stored in each individual flip-flop also appears at their respective output pins (Q0 =D0 ;Q1 = D1; Q2 = D2 Q3 = B3). This indicates that both data storage as well as data recovery occur at a single (and at the same) clock pulse in PIPO registers.

Truth table for PIPO shift register :



Waveform for PIPO shift registers :



**Why PIPO:**

* The PIPO shift register is mainly used to add time delay to digital circuits.
* PIPO Shift registers are used for converting data and also to shift the data from left to right and right to left.
* It is used for storing the data. These types of shift registers are also used for data storage, manipulation & data transfer.